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McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 12/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,451	NGO ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-19* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Amendment filed on 11/16/2004.

Currently, claims 12-19 and newly added claim 20 are pending. Claims 1-11 have been withdrawn from consideration.

Claim Objections

Claim objections have been withdrawn.

Claim Rejections - 35 USC § 112

The Claim rejections under 112 have be addressed. Rejection is removed.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alluri et al. (U.S. Patent No. 6,518,070 filed 5/17/2000) in view of Cheung (U.S. Patent No. 5,693,566 patented 12/2/1997).

Alluri shows the device substantially as claimed in Figs. 2-3 and corresponding text as: a transistor having gate structure (27) over a substrate (20) with a gate dielectric layer (26) therebetween (Fig. 2) (col. 2, lines 12-28); an interlayer dielectric (29) over the transistor and substrate; and a silicon-rich silicon oxide layer (32), on an upper surface of the interlayer dielectric (29) (Fig. 3) (col. 2, lines 12-45) (claim 12). Alluri teaches that the silicon-rich silicon oxide layer has a thickness of 400/ to 600/ (col. 2, lines 29-45) (claim 15).

Alluri lacks anticipation only in not explicitly teaching that: 1) the silicon-rich silicon oxide layer, has a refractive index (R.I.) greater than 1.6, on an upper surface of the interlayer dielectric (claim 12); 2)the silicon-rich silicon oxide layer has a R.I. greater than 1.7 (claim 13); 3)the silicon-rich silicon oxide layer has a R.I. of 1.7 to 2.0 (claim 14);

Cheung teaches the formation of silicon-rich silicon oxide having a refractive index of greater than 1.6, used as a liner to shield devices from moisture (col. 3, lines 17-30). As Cheung explains, an increase in silicon in a silicon oxide layer causes the index of refraction to increase as well. The index of refraction is 1.46 to 1.5, (col. 3, lines 30-33). Generally, Cheung teaches that in order for the silicon-rich silicon oxide layer to be reliable, the index of refraction should be higher than 1.6, (col. 3, lines 33-38). The increased reliability ensures that the underlying devices are optimally shielded from moisture.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the device shown in Alluri, by implementing the process

of forming a silicon-rich silicon oxide with a refractive index greater than 1.6 (which also includes the index of refraction being greater than 1.7 or being in the range of 1.7-2.0) as taught by Cheung, with the motivation that the silicon-rich silicon oxide has a refractive index greater than 1.6, it will shield the device from moisture and prevent the unintentional oxidation of underlying elements.

4. Claims 16-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Alluri et al. (U.S. Patent No. 6,518,070 filed 5/17/2000) in view of Cheung (U.S. Patent No. 5,693,566 patented 12/2/1997) as applied to claim 12 above, and further in view of Weimer (U.S. Patent No. 6, 559,007 filed 4/6/2000) and Wolf et al. (pg. 398 copyright 1986) .

Alluri and Cheung show the method substantially as claimed and as described in the preceding paragraphs. Additionally, Alluri teaches a generalized process to protect a transistor structure in a memory device.

Alluri and Cheung lack anticipation only in not explicitly teaching that: 1) the gate structure comprises: a tunnel oxide as the gate dielectric layer on the substrate; a floating gate electrode on the tunnel oxide; an interpoly dielectric comprising an oxide/nitride/oxide (ONO) stack on the floating gate; and a control gate electrode on the interpoly dielectric (claim 16); 2) silicon oxide spacers are formed on side surfaces of the gate structure (claim 17); 3) a layer of silicon nitride is formed on an upper surface of the gate structure and on the silicon oxide sidewall spacers (claim 18); and 4) the interlayer dielectric comprises a boron-phosphorus-doped silicate glass (BPSG) (claim 19).

Weimer teaches in Fig. 2 a similar semiconductor device that has the following features: a tunnel oxide (30) as the gate dielectric layer on the substrate(20)(col. 4 lines 3-20); a floating gate electrode (50) on the tunnel oxide (col. 4, line 62- col. 5, line 5); an interpoly dielectric comprising an oxide/nitride/oxide (ONO) stack (60)on the floating gate (col. 5, lines 6-15); and a control gate electrode (70) on the interpoly dielectric (col. 5 ,lines 16-23) (claim 16). Weimer teaches in Fig. 2, that, insulating spacers (90a and b) are formed on side surfaces of the gate structure (silicon oxide is a known and widely used insulating material)(col. 5, lines 24-31) (claim 17). Weimer teaches in Fig. 2 that, a layer of silicon nitride (92) is formed on an upper surface of the gate structure and on the silicon oxide sidewall spacers (col. 5, lines 32-54)(claim 18); Weimer also teaches that the interlayer dielectric comprises a boron-phosphorus-doped silicate glass (BPSG) (94)(col. 6, lines 1-8)(claim 19). The gate structure in Weimer eliminates OH molecules from diffusing into the tunnel oxide causing degradation of data retention and to minimize finite soft error rates.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination shown in Alluri and Cheung, by replacing the generic transistor structure of Alluri with the transistor structure of Weimer, with the motivation the silicon-rich silicon oxide layer will shield the transistor structure of Weimer from moisture and prevent the unintentional oxidation of underlying elements.

Wolf teaches the formation of silicon oxide spacers used to prevent the gate and source/drain areas from being electrically connected (pg. 398, lines 5-7).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, for the insulating spacers in the method of Alluri and Cheung as modified by Weimer to be made of silicon oxide, with the motivation that, the silicon oxide spacers will prevent the gate and source/drain areas from being electrically connected. Additionally, silicon oxide is a known and widely used insulating material that is utilized often in the production of sidewall spacers.

Response to Arguments

5. Applicant's arguments filed 11/16/2004 have been fully considered but they are not persuasive. The examiner views the arguments as not persuasive for the following reasons: A) layer (32) of Alluri is shown in Fig. 3 and in at least one embodiment is said to be made of a silicon-rich silicon oxide; B) the percentage of atomic concentration of semiconductor material is vital to this discussion and while Alluri does not make this clear the supporting teaching of Chueng makes up for the gap in teaching; and C) Chueng is used for its teaching that the increase in silicon in the silicon oxide raises the R.I. greater than 1.6, which lends support to the validity of discussing the atomic concentration of Alluri.

6. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re*

Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the properties of silicon-rich silicon oxide are the items Chueng is asked to teach. Alluri provides enough teaching in the direction of the claimed invention where it only lacks the teaching of silicon-rich silicon oxide having an R.I. of 1.6 or higher. The teaching of Chueng is used to illuminate the teaching of Alluri , in regards to layer (32), with the added support that Chueng's silicon-rich silicon oxide protects underlying elements which is what the claims as written address.

7. In response to applicant's argument that the examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).

Allowable Subject Matter

8. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...wherein the silicon-rich silicon oxide is substantially opaque to UV radiation, as required by claim 20 as it depends on claim 16.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F. Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WLL
December 22, 2004

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800